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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/018,180 | 09/09/2002 | Michael Offenberg | 10191/2083 | 8538 |

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| EXAMINER | |
|---|---|
| ANDERSON, MATTHEW A | |
| **ART UNIT** | **PAPER NUMBER** |
| 1722 | |

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/018,180 | OFFENBERG ET AL. | |
| | Examiner | Art Unit | |
| | Matthew A. Anderson | 1722 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 10,12-15,17-18 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Clark et al. (US 6,067,858).

Clark et al. discloses a micro-machined vibratory rate gyroscope as described in the abstract to consist of a substrate and a vibratory structure (i.e. a functional plane). Figs. 24A-24G show the steps of the fabrication and the structure obtained. In Fig. 24 A, described in cols. 23 and 24, a single-crystalline silicon substrate is used. This substrate has oxide and polysilicon layers added. The polysilicon is patterned. A second substrate is processed as described in Fig. 24B. The wafer is described as Si on insulator (SOI) and has a oxide layer sandwiched between two single-crystal silicon layers. A trench is formed in the single-crystal Si forming the functional plane (i.e. the vibration sensor) . Then, as shown in Fig. 24C the two substrates are bonded together and thinned to form the structure of Fig. 24D. In Fig. 24 E and 24F, integrated circuit processing is shown forming bonding pads (634) which may be conductive gold (col.24

lines 10-15). In Fig. 24 G , the final structure is shown after a capping substrate of glass or oxidized Si (640) is bonded. The functional plane (502 in Fig. 24G), the single-crystal Si substrate (602) of the covering plane (504), and printed circuit traces (606) of poly-Si on the covering plane are shown. The covering plane includes monocrystalline Si (aka single crystalline Si) with polysilicon thereon.

The examiner notes the product by process claims 10, 12-15, 17-18. The examiner notes that the product of Clark et al. appears to be the same as that claimed despite the lack of a simultaneous (i.e. at the same time) deposition of polycrystalline-silicon and monocrystalline-silicon in the process of making Clark et al.'s product.

Fig. 24 G of Clark et al. discloses a structure seemingly identical to that claimed. Although the applicant seeks to limit the process of Si deposition used to be simultaneous for both mono-crystalline and poly-crystalline Si, there is no apparent physical reason why these steps could not be sequential.

In the event that any differences can be shown for the product-by-process claims 10,12-15,17-18, as opposed to the product taught by the Clark et al. reference, such differences would have been obvious to one of ordinary skill in the art as a routine modification of the product in the absence of a showing of unexpected results; see also *In re Thorpe* , 227 USPQ 964 (Fed Cir. 1985).

## *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 11, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 6,067,858) in view of Wolf et al. (Silicon Processing for the VLSI Era Volume1: Processing Technology, Lattice Press, Sunset Beach, CA,USA, pp. 151-156, 1986.).

Clark is described above.

Clark does not disclose a functional plane consisting of epitaxial growth layers on of monocrystalline and polycrystal Si.

Wolf et al. discloses structures formed by epitaxial deposition of both single-crystalline and poly-crystalline Si. Wolf discloses simultaneous mono-crystalline and poly-crystalline deposition of Si on page 155 (see b in Fig. 28).

It would have been obvious to combine the discloses of Clark et al. and Wolf et al. to one of ordinary skill in the art at the time of the invention because Wolf et al. discloses known epitaxial structures and Clark et al. suggests (col. 24 lines 1-10) using conventional techniques (and thus structures) to form the micro-mechanical device.

In respect to claim 11, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form epitaxial monocrystalline and polysilicon structures because such conventional structures were known in the art and such conventional structure were suggested for use by Clark et al.

In respect to claim 19, it would have been obvious to one of ordinary skill in the art at the time of the present invention to produce a micro-mechanical component by providing a substrate, a functional plane on the substrate, a covering plane on the micro-mechanical functional plane, providing on the functional plane regions for polycrystal and monocrystal growth, epitaxially depositing poly and mono crystalline Si at the same time on the functional plane and providing a circuit trace on the covering plane because Clark et al. suggests (col. 24 lines 1-10) using conventional techniques (and thus structures) to form the micro-mechanical device and Wolf et al. discloses the simultaneous deposition of poly and mono crystalline Si in order to form conventional structures.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 6,067,858) in view of Sliwa et al. (US 5,075,253).

Clark does not disclose flip chip connection elements in the printed circuit trace plane.

Sliwa et al. discloses flip-chip structures formed on IC devices. The flip-chip structures are described as conventional for solder points to allow integration of the IC device into a larger device. ( see Fig. 17 and the description in col. 23 lines 35-55)

It would have been obvious to combine the discloses of Clark et al. and Sliwa et al. to one of ordinary skill in the art at the time of the invention because Sliwa et al. discloses known conventional flip-chip structures and Clark et al. suggests (col. 24 lines 1-10) using conventional techniques (and thus structures) to form the micro-mechanical device. Motivation for combination is the suggested utility of integration in Sliwa et al.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to include flip-chip structures because such would allow the device to be connected to further devices to form more complex devices.

### *Response to Arguments*

7. Applicant's arguments filed 4/14/2005 have been fully considered but they are not persuasive.

The examiner notes the 'comprising' transitional phrase which allows other unclaimed elements to be present.

The argument that the Wolf reference does not apply to the present invention since it has to do with Si used in VLSI is not persuasive. Wolf et al. does indeed disclose the individual deposition and etching steps recited by the applicant. Wolf et al. has been combined with Clark which does describe micromechanical components.

The argument that the process of Wolf et al. would necessarily produce structurally different product is not persuasive. The applicant has claimed a product by process and the examiner notes that a sequential process would seem to produce equivalent results. The size of the layers is an obvious design choice depending on the function of the component made.

The argument that the combination of Sliwa et al. is technically impossible is not convincing. References do not need to be physically combinable [*In re Etter* 225 USPQ 1 Fed Cir. 1985 en banc)]. Sliwa et al suggests the use of flip chip technology for easy and useful integration.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Anderson whose telephone number is (571) 272-1459. The examiner can normally be reached on M-F, 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on (571) 272-1166. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAA
July 24, 2005

GREGORY MILLS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700